What is claimed is:

1. A liquid crystal display apparatus comprising:

a liquid crystal display panel comprising a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to said transistors, said transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for respectively activating the liquid crystal cells; and

a driving circuit for successively generating a plurality of write-in voltages of a line signal of a video frame at end points of said column lines, successively selecting each of said row lines and supplying said write-in voltages from said end points of the column lines to the liquid crystal cells of the selected row line for a period corresponding to a geometric distance from the selected row line to said end points.

2. The liquid crystal display apparatus of claim 1, wherein said driving circuit comprises:

a buffer memory for storing said video frame;

a timing controller for generating first and second timing signals;

a column driver for receiving a line signal from said memory, converting said line signal to said write-in voltages and supplying said write-in voltages to said column lines in response to said first timing signal; and

a row driver for successively selecting each of said row lines for an interval between successive ones of said second timing signal and supplying said write-in voltages to the liquid crystal cells of the selected row line for a write-in period which runs from said first timing signal to said second timing signal,

said timing controller generating said first timing signal at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver and generating said second timing signal at

said increasingly variable intervals.

3. The liquid crystal display apparatus of claim 2, wherein said write-in period is increasingly variable from a nominal value.

4. The liquid crystal display apparatus of claim 2, wherein said timing controller comprises:

a memory for storing a plurality of additive values, each of the additive values corresponding to a geometric distance from the selected row line to said column driver;

a line counter for incrementing a count number in response to a line signal and reading an additive variable from said memory corresponding to the count number;

an adder for summing the read variable with a constant value; and

variable-rate pulse generating means for producing each of said first and second timing signals at intervals corresponding to an output signal of said adder.

5. The liquid crystal display apparatus of claim 1, wherein said driving circuit comprises:

a timing controller for generating a first, second and third timing signals;

a column driver for converting a line signal to said write-in voltages and supplying said write-in voltages to said column lines in response to the first timing signal;

a row driver for successively selecting one of said row lines for an interval between successive ones of said second timing signal and supplying said write-in voltages to the liquid crystal cells of the selected row line for a write-in period which runs from said first timing signal to said third timing signal,

said timing controller generating each of said first and second timing signals at constant intervals and generating said third timing signal at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver.

6. The liquid crystal display apparatus of claim 5, wherein said write-in period is variable from a less-than-nominal value to a nominal value.

7. The liquid crystal display apparatus of claim 5, wherein said timing controller comprises:

a memory for storing a plurality of subtractive values, each of the subtractive values corresponding to a geometric distance from the selected row line to said column driver;

a line counter for incrementing a count number in response to a line signal and reading a subtractive value from said memory corresponding to the count number;

a subtractor for subtracting the read subtractive value from a constant value;

constant-rate pulse generating means for producing each of said first and second timing signals at constant intervals; and

variable-rate pulse generating means for producing said third timing signal at intervals corresponding to an output signal of said subtractor.

8. The liquid crystal display apparatus of claim 1, wherein said driving circuit comprises:

a buffer memory for storing said video frame;

a timing controller for generating first, second, third, fourth and fifth timing pulses;

a column driver for receiving a line signal from said memory, converting said line signal to said write-in voltages and supplying said write-

in voltages to said column lines in response to said first timing signal during a first portion of a frame interval and in response to said fourth timing signal during a second portion of the frame interval;

a row driver for successively selecting one of said row lines for an interval between successive ones of said second timing signal during said first portion of the frame interval and supplying said write-in voltages to the liquid crystal cells of the selected row line for a write-in period which runs from said first timing signal to said third timing signal, successively selecting one of said row lines for an interval between successive ones of said fifth timing signal during said second portion of the frame interval and interval, and supplying said write-in voltages to the liquid crystal cells of the selected row line for a write-in period which runs from said fourth timing signal to said fifth timing signal,

said timing generator generating, during said first portion of the frame interval, each of said first and second timing signals at constant intervals and said third timing signal at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver and generating, during said second portion of the frame interval, each of said fourth and fifth timing signals at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver.

9. The liquid crystal display apparatus of claim 8, wherein said write-in period of said first portion of the frame interval is increasingly variable from a less-than-nominal value to a nominal value and the said write-in period of said second portion of the frame interval is increasingly variable from said nominal value.

10. The liquid crystal display apparatus of claim 8, wherein said timing controller comprises:

a memory for storing a plurality of subtractive values and a plurality

of additive values, each of said subtractive and additive values corresponding to a geometric distance from the selected row line to said column driver;

a line counter for incrementing a count number in response to a line signal and reading one of said subtractive values from said memory corresponding to the count number during said first portion of the frame interval and reading one of said additive values from said memory corresponding to the count number during said second portion of the frame interval;

a subtractor for subtracting from a constant value the subtractive value which is read from said memory during said first portion of the frame interval;

an adder for summing said constant value with the additive value which is read from said memory during said second portion of the frame interval;

constant-rate pulse generating means for producing each of said first and second timing signals at constant intervals; and

variable-rate pulse generating means for producing said third timing signal at intervals corresponding to an output signal of said subtractor and producing each of said fourth and fifth timing signal at intervals corresponding to an output signal of said adder.

11. A method of driving a liquid crystal display, wherein the liquid crystal display panel comprises a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to said transistors, said transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for respectively activating the liquid crystal cells, the method comprising the steps of:

a) generating a plurality of write-in voltages of a line signal of a video frame so that the write-in voltages appear at end points of said column

lines;

b) successively selecting one of said row lines; and

c) successively supplying said write-in voltages from said end points of the column lines to the liquid crystal cells of the selected row line for a write-in period corresponding to the geometric distance from the selected row line to said end points.

12. The method of claim 11, wherein step (a) comprises the step of buffering said line signal in a memory and wherein step (c) comprises the step of increasingly varying said write-in period from a nominal value as a function of said geometric distance.

13. The method of claim 11, wherein step (c) comprises the step of increasingly varying said write-in period as a function of said geometric distance in a range from a less-than-nominal value to a nominal value.

14. The method of claim 11, wherein step (a) comprises the step of buffering said line signal in a memory and wherein step (d) comprises the step of increasingly varying said write-in period as a function of said geometric distance in a range from a less-than-nominal value to a nominal value during a first portion of a frame interval and increasingly varying said write-in period as a function of said geometric distance from the nominal value.

15. A driving circuit for a liquid crystal display which comprises a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to said transistors, said transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for respectively activating the liquid crystal cells, the driving circuit comprising means for successively generating a plurality of write-in voltages

of a line signal of a video frame at end points of said column lines, successively selecting each of said row lines and supplying said write-in voltages from said end points of the column lines to the liquid crystal cells of the selected row line for a period corresponding to a geometric distance from the selected row line to said end points.

16. The driving circuit of claim 15, wherein said means comprises:

a buffer memory for storing said video frame;

a timing controller for generating first and second timing signals;

a column driver for receiving a line signal from said memory, converting said line signal to said write-in voltages and supplying said write-in voltages to said column lines in response to said first timing signal; and

a row driver for successively selecting each of said row lines for an interval between successive ones of said second timing signal and supplying said write-in voltages to the liquid crystal cells of the selected row line for a write-in period which runs from said first timing signal to said second timing signal,

said timing controller generating said first timing signal at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver and generating said second timing signal at said increasingly variable intervals.

17. The driving circuit of claim 16, wherein said write-in period is increasingly variable from a nominal value.

18. The driving circuit of claim 16, wherein said timing controller comprises:

a memory for storing a plurality of additive values, each of the additive values corresponding to a geometric distance from the selected row line to said column driver;

a line counter for incrementing a count number in response to a line signal and reading an additive variable from said memory corresponding to the count number;

an adder for summing the read variable with a constant value; and

variable-rate pulse generating means for producing each of said first and second timing signals at intervals corresponding to an output signal of said adder.

19. The driving circuit of claim 15, wherein said driving circuit comprises:

a timing controller for generating a first, second and third timing signals;

a column driver for converting a line signal to said write-in voltages and supplying said write-in voltages to said column lines in response to the first timing signal;

a row driver for successively selecting one of said row lines for an interval between successive ones of said second timing signal and supplying said write-in voltages to the liquid crystal cells of the selected row line for a write-in period which runs from said first timing signal to said third timing signal,

said timing controller generating each of said first and second timing signals at constant intervals and generating said third timing signal at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver.

20. The driving circuit of claim 19, wherein said write-in period is variable from a less-than-nominal value to a nominal value.

21. The driving circuit of claim 19, wherein said timing controller comprises:

a memory for storing a plurality of subtractive values, each of the subtractive values corresponding to a geometric distance from the selected row line to said column driver;

a line counter for incrementing a count number in response to a line signal and reading a subtractive value from said memory corresponding to the count number;

a subtractor for subtracting the read subtractive value from a constant value;

constant-rate pulse generating means for producing each of said first and second timing signals at constant intervals; and

variable-rate pulse generating means for producing said third timing signal (VOE) at intervals corresponding to an output signal of said subtractor.

22. The driving circuit of claim 15, wherein said means comprises:

a buffer memory for storing said video frame;

a timing controller for generating first, second, third, fourth and fifth timing pulses;

a column driver for receiving a line signal from said memory, converting said line signal to said write-in voltages and supplying said write-in voltages to said column lines in response to said first timing signal during a first portion of a frame interval and in response to said fourth timing signal during a second portion of the frame interval;

a row driver for successively selecting one of said row lines for an interval between successive ones of said second timing signal during said first portion of the frame interval and supplying said write-in voltages to the liquid crystal cells of the selected row line for a write-in period which runs from said first timing signal to said third timing signal, successively selecting one of said row lines for an interval between successive ones of said fifth timing signal during said second portion of the frame interval and interval, and supplying said write-in voltages to the liquid crystal cells of the selected

row line for a write-in period which runs from said fourth timing signal to said fifth timing signal,

said timing generator generating, during said first portion of the frame interval, each of said first and second timing signals at constant intervals and said third timing signal at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver and generating, during said second portion of the frame interval, each of said fourth and fifth timing signals at intervals increasingly variable as a function of the geometric distance from the selected row line to said column driver.

23. The driving circuit of claim 22, wherein said write-in period of said first portion of the frame interval is increasingly variable from a less-than-nominal value to a nominal value and the said write-in period of said second portion of the frame interval is increasingly variable from said nominal value.

24. The driving circuit of claim 22, wherein said timing controller comprises:

a memory for storing a plurality of subtractive values and a plurality of additive values, each of said subtractive and additive values corresponding to a geometric distance from the selected row line to said column driver;

a line counter for incrementing a count number in response to a line signal and reading one of said subtractive values from said memory corresponding to the count number during said first portion of the frame interval and reading one of said additive values from said memory corresponding to the count number during said second portion of the frame interval;

a subtractor for subtracting from a constant value the subtractive value which is read from said memory during said first portion of the frame

interval;

an adder for summing said constant value with the additive value which is read from said memory during said second portion of the frame interval;

constant-rate pulse generating means for producing each of said first and second timing signals at constant intervals; and

variable-rate pulse generating means for producing said third timing signal at intervals corresponding to an output signal of said subtractor and producing each of said fourth and fifth timing signals at intervals corresponding to an output signal of said adder.